Sem IV C-scheme KT (INFT) winter 2025 12/12/25

TIME: 3 HRS MARKS:80

N.B. 1. Question No 1 is compulsory.
2. Solve any **three** questions out of the remaining five questions.
3. Assume suitable data if necessary.
4. Figures to the right indicate marks.

Q1. Attempt any 4 sub questions

a) Minimize the Boolean function using K-map (4 variables): (5)
$F(A, B, C, D) = \Sigma(0, 2, 5, 7, 8, 10, 13, 15)$.
Implement the simplified function using logic gates.
b) Discuss various assembler directives of 8086 microprocessor. (5)
c) What is instruction pipelining? Explain six stage pipelining. (5)
d) Draw the flowchart of unsigned binary restoring division algorithm. (5)
e) Explain computer memory hierarchy. (5)

Q2. a) Explain the working of a Master–Slave JK Flip-Flop. Derive its truth table and justify how it overcomes the race-around condition seen in a simple JK Flip-Flop. (10)
b) Describe various addressing modes of 8086 microprocessor with suitable example. (10)

Q3 a) Represent the number (- 0.0625) in single and double precision IEEE 754 binary floating point representation formats. (10)
b) What are Pipeline Hazards? Explain different types of Pipeline Hazards. (10)

Q4 a) Draw and Explain Maximum mode of 8086 microprocessor. (10)
b) Draw the flowchart of Booths algorithm and multiply (-7)*(5) using Booths algorithm. (10)

Q5. a) Explain Interrupt driven I/O and Programmed I/O. (10)
b) Consider a direct mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB.
1. Find- Find TAG, BLOCK, WORD using direct mapping
2. Find TAG, WORD using associative mapping
3. Find TAG, SET WORD using 4 way set associative mapping (10)

Q6 Write notes on (any two) (20)
a) Full subtractor
b) DMA.
c) Instruction execution cycle with interrupt processing.
